**MAIN VHDL CODE**

--------------------------------------------------------------------

-- Engineer: S. A. C. Dilhani Maddumage

-- Create Date: 02:06:34 07/05/2021

-- Design Name: 4 Bit Universal Shift Register

-- Module Name: universal\_shift\_register\_4bit - Behavioral

-- Project Name: Advanced Digital Design Assignment 01

---------------------------------------------------------------------

**library** IEEE**;**

**use** IEEE**.**STD\_LOGIC\_1164**.ALL;**

**entity** universal\_shift\_register\_4bit **is**

**port** **(** sir **:** **in** std\_logic**;** --serial input right

sil **:** **in** std\_logic**;** --serial input left

clk **:** **in** std\_logic**;** --clock input

rst **:** **in** std\_logic**;** --reset input

d **:** **in** std\_logic\_vector **(**3 **downto** 0**);** --parallel data inputs

s **:** **in** std\_logic\_vector **(**1 **downto** 0**);** --selecting inputs

q **:** **out** std\_logic\_vector **(**3 **downto** 0**)** **);** --data outputs

**end** universal\_shift\_register\_4bit**;**

**architecture** Behavioral **of** universal\_shift\_register\_4bit **is**

**signal** t**:** std\_logic\_vector **(**3 **downto** 0**);**

**begin**

**process** **(**sir**,**sil**,**d**,**s**,**clk**,**rst**)**

**begin**

**if** rst**=**'0' **then**

t**<=**"0000"**;** --set temp to 0000

q**<=**"0000"**;** --set data output to 0000

**elsif** **(**clk**=**'1' **and** clk' **event)** **then**

**case** s **is**

**when** "01" **=>** --shift left

t**<=**d**;** --load parallel inputs to the temp

t**(**3 **downto** 1**)** **<=** t**(**2 **downto** 0**);** --load temp(0) temp(1) temp(2) in to temp(1) temp(2) temp(3) respectively

t**(**0**)** **<=** sil**;** --load serial input right into the temp(0)

q**<=**t**;** --load temp in to data output

**when** "11" **=>** --parallel loading

t**<=**d**;** --load parallel inputs to the temp

q**<=**t**;** --load temp to data output

**when** "10" **=>** --shift right

t**<=**d**;** --load parallel inputs to the temp

t**(**2 **downto** 0**)** **<=** t**(**3 **downto** 1**);** --load temp(1) temp(2) temp(3) in to temp(0) temp(1) temp(2) respectively

t**(**3**)** **<=** sir**;** --load serial input left into the temp(3)

q**<=**t**;** --load temp in to data output

**when** "00" **=>** --hold

temp**<=**temp**;** -- hold the temp

q**<=**temp**;** --load temp in to data output

**when** **others** **=>** **null;** --hold

**end** **case;**

**end** **if;**

**end** **process;**

**end** Behavioral**;**

**TEST BENCH**

--------------------------------------------------------------------

-- Engineer: S. A. C. Dilhani Maddumage

-- Create Date: 02:34:58 07/05/2021

-- Design Name: 4 Bit Universal Shift Register

-- Module Name: C:/ADD Assignment 01/universal\_shift\_register\_4bit/universal\_shift\_register\_4bit\_test\_bench.vhd

-- Project Name: universal\_shift\_register\_4bit

-- VHDL Test Bench Created by ISE for module: universal\_shift\_register\_4bit

--------------------------------------------------------------------

**LIBRARY** ieee**;**

**USE** ieee**.**std\_logic\_1164**.ALL;**

**ENTITY** universal\_shift\_register\_4bit\_test\_bench **IS**

**END** universal\_shift\_register\_4bit\_test\_bench**;**

**ARCHITECTURE** behavior **OF** universal\_shift\_register\_4bit\_test\_bench **IS**

-- Component Declaration for the Unit Under Test (UUT)

**COMPONENT** universal\_shift\_register\_4bit

**PORT(**

sir **:** **IN** std\_logic**;**

sil **:** **IN** std\_logic**;**

clk **:** **IN** std\_logic**;**

rst **:** **IN** std\_logic**;**

d **:** **IN** std\_logic\_vector**(**3 **downto** 0**);**

s **:** **IN** std\_logic\_vector**(**1 **downto** 0**);**

q **:** **OUT** std\_logic\_vector**(**3 **downto** 0**)**

**);**

**END** **COMPONENT;**

--Inputs

**signal** sir **:** std\_logic **:=** '0'**;**

**signal** sil **:** std\_logic **:=** '0'**;**

**signal** clk **:** std\_logic **:=** '0'**;**

**signal** rst **:** std\_logic **:=** '0'**;**

**signal** d **:** std\_logic\_vector**(**3 **downto** 0**)** **:=** **(others** **=>** '0'**);**

**signal** s **:** std\_logic\_vector**(**1 **downto** 0**)** **:=** **(others** **=>** '0'**);**

--Outputs

**signal** q **:** std\_logic\_vector**(**3 **downto** 0**);**

-- Clock period definitions

**constant** clk\_period **:** time **:=** 10 ns**;**

**BEGIN**

-- Instantiate the Unit Under Test (UUT)

uut**:** universal\_shift\_register\_4bit **PORT** **MAP** **(**

sir **=>** sir**,**

sil **=>** sil**,**

clk **=>** clk**,**

rst **=>** rst**,**

d **=>** d**,**

s **=>** s**,**

q **=>** q

**);**

-- Clock process definitions

clk\_process **:process**

**begin**

clk **<=** '0'**;**

**wait** **for** clk\_period**/**2**;**

clk **<=** '1'**;**

**wait** **for** clk\_period**/**2**;**

**end** **process;**

-- Stimulus process

stim\_proc**:** **process**

**begin**

--reset

rst**<=**'0'**;**

**wait** **for** 100 ns**;**-- hold at same state for 100 ns.

--hold

rst**<=**'1'**;**

**wait** **for** 100 ns**;**

d**<=**"1101"**;**

s**<=**"00"**;**

**wait** **for** 100 ns**;**-- hold selection at same state for 100 ns.

--parallel loading

s**<=**"11"**;**

**wait** **for** 100 ns**;**-- hold selection at same state for 100 ns.

--shift right

s**<=**"10"**;**

sir**<=** '1'**;**

**wait** **for** 100 ns**;**-- hold selection at same state for 100 ns.

--shift left

s**<=**"01"**;**

sil**<=** '0'**;**

**wait** **for** 100 ns**;**-- hold selection at same state for 100 ns.

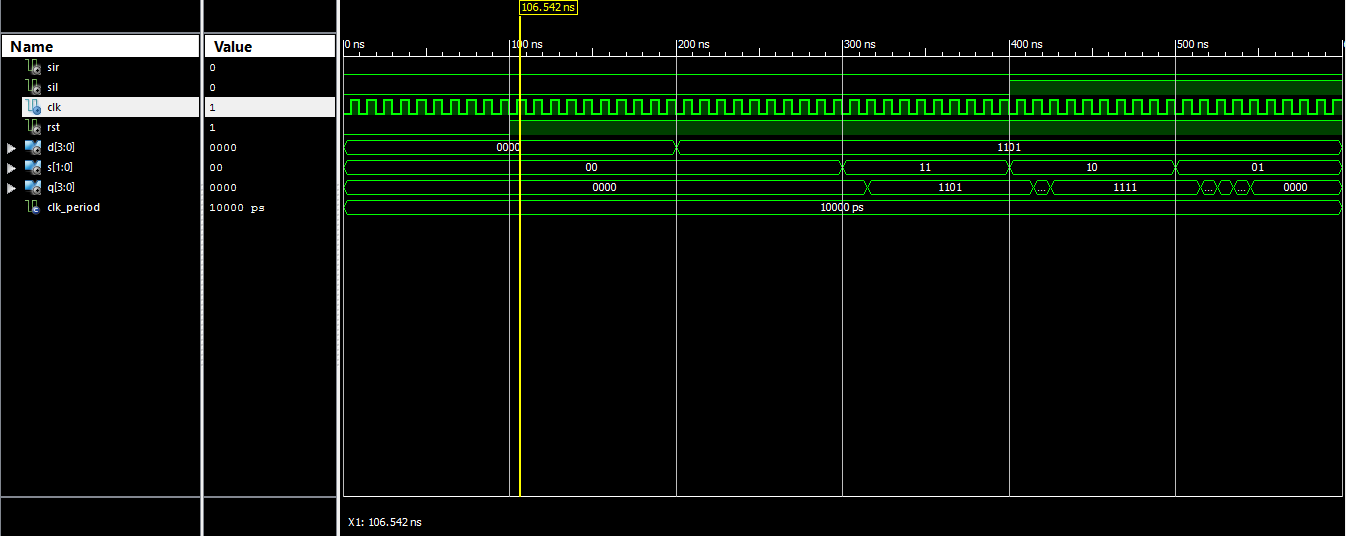
**wait;**

**end** **process;**

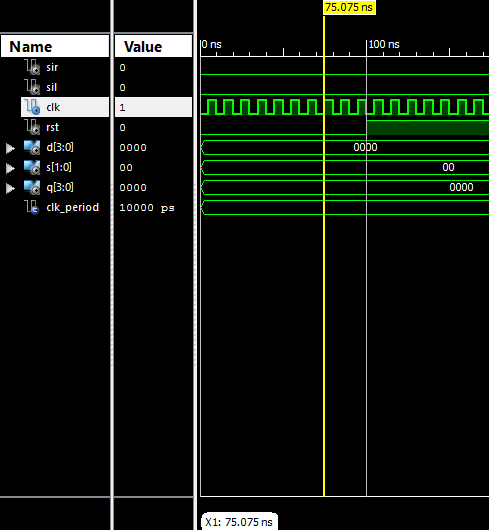
**END;**

**SIMULATION RESULTS**

**FULL WAVEFORM**



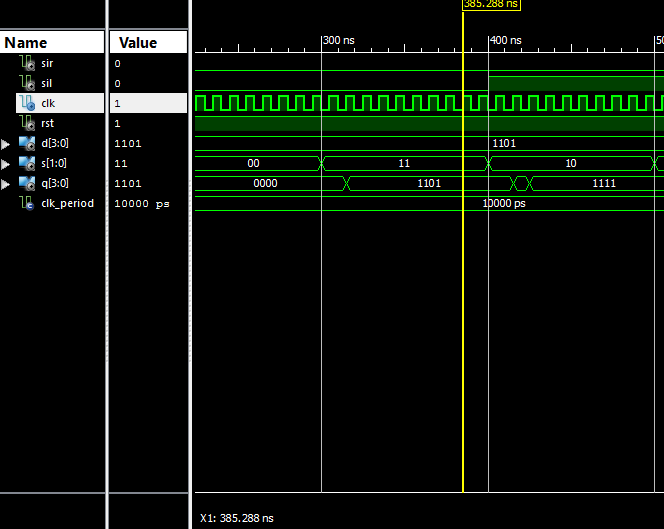
**RESET (UNTILL 100NS)**



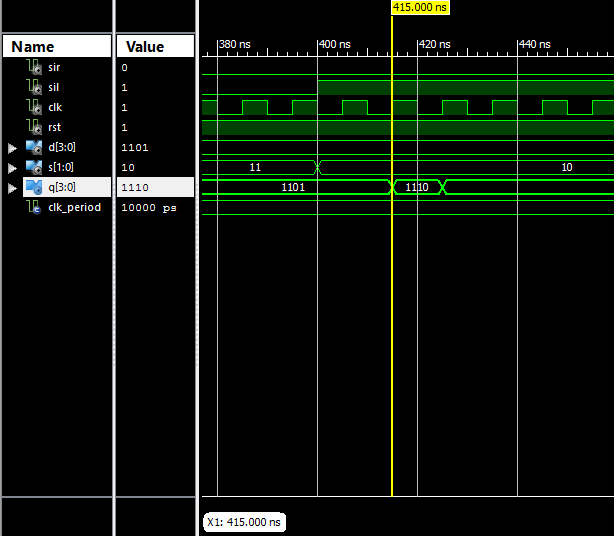
**HOLD 0000 FORM 100NS TO 300NS**



**PARALLEL LOADING AT 300NS**



**SHIFT RIGHT AT 315NS AND 325NS**



**SHIFT LEFT AT 515NS 525NS, 535, 545NS**

